AMENDMENTS TO THE CLAIMS

A detailed listing of all claims that are, or were, in the present application, irrespective of whether the claim(s) remains under examination in the application are presented below. The claims are presented in ascending order and each includes one status identifier. Those claims not cancelled or withdrawn but amended by the current amendment utilize the following notations for amendment: 1. deleted matter is shown by strikethrough for six or more characters and double brackets for five or less characters; and 2. added matter is shown by underlining.

1. (Previously Presented) A method of processing a communication in a computer system having at least one input interface and at least one output interface for respectively receiving a communication and outputting the communication after processing, the method comprising:

providing at least a first and a second central processing unit (CPU) coupled to respective first and second private memories, the first and second CPUs capable of executing one or more processes under control of an operating system, each process operative to generate at least a portion of a response to the communication;

configuring a communications interconnection mechanism for operatively linking the CPUs, a shared memory, the input interface, the output interface and a system I/O bus for data communication there between;

receiving the communication at the input interface;

directly storing the communication received in the shared memory using the communication interconnection mechanism and independently of the system I/O bus;

providing the communication stored in the shared memory directly to at least one of the first and second CPUs over the communication interconnection mechanism without causing an interrupt of the operating system and independently of the system I/O bus;

executing at least one of the one or more processes on at least one of the first and second CPUs to generate at least a portion of the response to the communication;

receiving the generated portion of the response to the communication from the at least first and second CPUs in the respective private memories associated with each of the first and second CPUs;

storing in an outgoing storage the response comprising the portion of the responses generated at each of the first and second CPUs; and

providing the response directly to the output interface without causing an interrupt to the operating system and independently of the system I/O bus.

2. (Currently Amended) The method of claim 1 wherein:

the communication is stored in the shared storage accessible to the first and second CPUs;

the response is stored in one of the first and second private memories [[not]] inaccessible by respective ~~at least one of~~ the ~~first~~ second and ~~second~~ the first CPUs; and

the response is provided from the one of the first and second CPUs.

3. (Previously Presented) The method of claim 2:

additionally comprising assigning the communication received to at least one of a plurality of queues in the shared memory, the plurality of queues each corresponding to a different one of the first and second CPUs; and

wherein the providing the communication step comprises providing the communication to at least one of the first and second CPUs corresponding to the at least one queue to which the communication was assigned.

4. (Original) The method of claim 3, wherein the assigning step is responsive to a prior communication.

5. (Original) The method of claim 3 wherein the assigning step is responsive to information contained in the communication.

6. (Previously Presented) The method of claim 1 wherein the response is additionally provided independently of the communication interconnection mechanism and the system I/O bus.

7. (Previously Presented) The method of claim 1 wherein the communication comprises a packet.

8. (Previously Presented) The method of claim 1 wherein the communication comprises an Ethernet frame.

9. (Previously Presented) The method of claim 1 wherein the communication comprises a storage device communication.

10. (Canceled)

11. (Currently Amended) A system for processing a communication, comprising:

an incoming communication interface having an incoming communication interface input and an incoming communication interface output, the incoming communication interface input operative for receiving the communication, the incoming communication interface output operative for providing at least a portion of the communication received at the incoming communication interface input;

a plurality of central processing units (CPUs) wherein each CPU is coupled to a private memory for exclusive access by the CPU and wherein each CPU is configured to run a process that executes in an operating system environment to generate at least a portion of a response communication;

a first storage operatively connected to an incoming interface manager and a shared memory interface, the shared memory interface communicatively coupled to the plurality of CPUs via a communications interconnection mechanism, the incoming interface manager having an input coupled to the incoming communication interface output, the incoming interface manager operative for directly storing the communication received at the incoming interface manager input into [[a]] the first storage independent of CPU intervention, the shared memory

interface operative to provide shared access to the shared memory by the plurarity of CPUs using the communications interconnection mechanism for retreiving at least a portion of the stored communication from the first storage and for providing the retreived communication to at least one of [[a]] the plurality of CPUs;

a plurality of second interfaces, each of the plurality of second interfaces corresponding and coupled to ~~a fewer than all~~ a unique one of the plurality of CPUs and having a second interface input for receiving a response to the communication from ~~at least~~ the unique one of the ~~at least one of the~~ plurality of CPUs and a second interface output for providing the response to a second storage coupled to [[an]] the second interface output; and

an outgoing interface manager ~~having~~ communicatively coupled to an outgoing interface manager input/ output ~~coupled to the second storage~~ and an outgoing communication interface the outgoing interface manager input/output being coupled to the second storage, the outgoing interface manager adapted for retrieving the response directly from the second storage ~~unaccompanied by~~ without causing an interrupt to be generated in the operating system environment and providing the response at [[an]] the outgoing communication interface ~~output~~.

12. (Currently Amended) The system of claim 11, wherein:

the second interface input coupled to at least one of the plurality of ~~entities~~ CPUs but coupled to fewer than all of the plurality of ~~entities~~ CPUs.

13. (Currently Amended) The system of claim 12, wherein:

the incoming interface manager is additionally for assigning the communication received to at least one of a plurality of queues in the first storage, the plurality of queues each corresponding to a different one of the ~~entities~~ plurality of CPUs; and

and wherein the first interface provides the communication by to at least one of the plurality of ~~entities~~ CPUs corresponding to the at least one queue to which the communication was assigned.

14. (Original) The system of claim 13, wherein the incoming interface manager assigns the communication responsive to a prior communication.

15. (Original) The system of claim 13 wherein the incoming interface manager assigns the communication responsive to information contained in the communication.

16. (Original) The system of claim 11 wherein the outgoing interface manager additionally retrieves the response from the second storage sinebusly.

17. (Original) The system of claim 11 wherein the communication comprises a packet.

18. (Original) The system of claim 11 wherein the communication comprises an Ethernet frame.

19. (Original) The system of claim 11 wherein the communication comprises a storage device communication.

20 - 31 (Canceled)

32. (Previously Presented) A computer system comprising:

at least one main processing unit including at least one private memory and at least one process, the private memory adapted to provide dedicated access to the at least one main processing unit, the process configured to execute under control of an operating system and processing at least a first portion of a communication received by the computer system into at least a portion of a response for storage in the at least one private memory;

an incoming shared memory operatively coupled to an input interface and a shared memory interface, the shared memory interface operatively coupled to the at least one main processing unit via a communications interconnection mechanism, the input interface operative to receive and store at least a portion of the communication in the incoming shared memory independently of the communications interconnection mechanism and independently of the operating system, the incoming shared memory operative to arbitrate shared access to the portion of the stored communication by the at least one main processing unit independently of the input interface and unaccompanied by an interrupt to the operating system; and

an outgoing shared memory operative to retrieve and selectively output the portion of the response form the private memory independently of the communications interconnection mechanism and unassisted by the operating system.

33. (Previously Presented) The computer system of claim 32 wherein the at least one main processing unit includes at least two central processing units (CPU)s configured for inter-processor communication over the communications interconnection mechanism.

34. (Previously Presented) The computer system of claim 32 wherein the incoming shared memory is a multi-port RAM capable of supporting concurrent write and read memory operations by the input interface and the shared memory interface respectively.

35. (Previously Presented) The computer system of claim 32 wherein the input interface comprises a direct memory access (DMA) controller.

36. (Previously Presented) The computer system of claim 32 further including software logic operative to generate software pointers that organize the incoming shared memory for writing to and reading from by the input interface and the shared memory interface respectively.

37. (Previously Presented) The computer system of claim 36 wherein the orgianized incoming shared memory has a circular buffer architecture.

38. (Previously Presented). A computer system comprising:

an input interface operably coupled to a communications transferring medium to receive an input communications therefrom ;

a shared memory coupled to the input interface and having a predefined number of physical storage locations for storing the input communications therein;

a memory map comprising updateable software pointers including a first portion of the software pointers that allocate at least a first portion of the physical storage locations for write operations and a second portion of the software pointers point to at least a second portion of the physical storage locations for read operations;

one or more processing units wherein each processing unit is operatively coupled to a private memory for exclusive use by the processing unit and configured to execute a process in a first operating system environment; and

a communications interconnection mechanism operably coupled to the one or more processing units and the shared memory via a shared memory interface, the communications interconnection mechanism operative to at least partially enable interprocessor communication and shared access to the shared memory by the one or more processing units wherein the input interface is adapted to perform the write operations and optionally update the software pointers, the one or more processing units configured to perform the read operations arbitrated by the shared memory interface such that each processing units reads input communications stored in non-overlapping regions of the second portion of the physical storage locations for processing into a response written to the private memory via the process associated with the processing unit, the memory map characterized in that the first portion of the physical storage locations for write

operations include physical storage locations devoid of input communications or storing input communications that have been read as a result of the read operations wherein the read and write operations avoid generating an interrupt to the first operating system environment and avoid inter-processor communication.

39. (Previously Presented) The system of claim 38 wherein the memory map is a circular buffer.

40 (Previously Presented) The system of claim 38 wherein the shared memory is a two port memory with a first port configured for read operations and a second port configured for write operations.

41. (Previously Presented) The system of claim 38 wherein portions of the input communications are associated with a transmission related characteristic that is related to a pre-assigned designator of a first one of the one or more processing units and wherein the portions of the input communications that match a pre-assigned designator are stored or retrieved as one or more units for processing by the associated processing unit.

42. (Currently Amended) A method for processing a communication in a computer system comprising the steps of:

providing an input interface to a communications medium;

coupling a shared memory to the input interface, the shared memory including one or more physical storage locations;

operatively coupling a plurality of processors and a plurality of private memories to a communications interconnection mechanism and coupling the communications interconnections mechanism to the shared memory to enable the plurality of processors to share access to the shared memory and enable each processor dedicated access to one of the plurality of private memories;

providing each processor with a process running under a first operating system;

updating a set of software pointers to at least a portion of the physical storage locations so that a portion of the shared memory is organized as a circular buffer;

receiving an input communication and storing it directly into the circular buffer at a first tail location of the circular buffer;

transferring [[an]] the input communication at a head of the circular buffer to one of the processing units;

executing the process to generate a response communication based upon the input communication transferred to the processing unit; and

storing the response in the private memory associated with the processing unit for transmission to the communications medium.

43. (Previously Presented) The method of claim 42 wherein the step of storing the response in the private memory further includes:

providing an output shared storage for retrieving and organizing the response from the private memroy into an output communication; and

transmitting the output communication to the communications medium.

44. (Previously Presented) A method for responding to an incoming communication comprising:

providing a plurality of processes executing under an operating system hosted by one or more central processing units (CPUs) wherein each CPU is coupled to a private memory for exclusive access by the CPU and each process is capable of generating a response by processing at least a portion of the incoming communication;

operatively coupling a system memory via a communications interconnection mechanism to the one or more CPUs and to an input interface adapted to receive the incoming communication;

generating and storing in hardware a plurality of software pointers allocating at least one writable location for writing to and at least one readable location for reading from the system memory;

directly writing at least a portion of the incoming communication to the at least one writable location unassisted by the operating system;

selectively allowing one of the plurality of processes to directly read at least the portion of the incoming communication from the at least one readable location avoiding interrupt generation to the operating system; and

processing the retrieved portion of the incoming communication using the selected process to generate and store a response in the private memory avoiding interprocessor communication between the one or more CPUs.

45. (Previously Presented) The system of claim 38 wherein the communication interconnection mechanism is a system bus.

46. (Previously Presented) The method of claim 44 wherein the communications interconnection mechanism is a system bus.